SESSION 18: FET MODELING AND NOVEL STRUCTURES

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Rapid performance advances continue to be made at microwave frequencies with amplifiers, mixers, that use field effect transistors as their active element. Significant progress has been made in modeling these devices for determining the accurate equivalent circuit element values for GaAs FETs. First three papers in this session report the progress in modeling of the GaAs FETs for determining the equivalent circuit elements values which serves as an invaluable aid for device diagnostics and for the development of amplifiers, mixers, etc.

The first paper by Curtice & Camisa describes a procedure for producing accurate and unique equivalent circuit models for carrier mounted GaAs FETs. The procedure incorporates zero drain-source bias S-parameter tests as well as Fukui-type measurements. The second paper by Gilmore and Rosenbaum describes a modified harmonic balance approach applied to a GaAs FET model to simulate two tone intermodulation distortion and multiple signal suppression in MESFET amplifiers and mixers. An analysis based on a lumped element quasi-static FET equivalent circuit, developed by Maas, is described in the third paper. The analysis is useful for harmonic mixers, upconverters for mixers, etc.

The last three papers report the progress being made in the development of novel FET structure for low noise and high power applications. A new low-noise FET based on the N-AlGaAs/GaAs selectively doped structure has been developed by K. Ohata et al and is reported in the fourth paper. The FET has a planar structure with a p^+-gate and a close space structure between gate and source in order to have small resistance. The 0.5 μm gate FET exhibited marked room temperature performance of 310 ms/mm transconductance and 1.2 dB noise figure with 11.7 dB associated gain. A new in-package matching technique has been developed by Magalhas et al which utilizes GaAs matching circuits and is presented in the 5th paper of the session. This technique allows individual optimization of devices for high power or efficiency and is economical of development time while retaining most of the advantages of monolithic integration. A GaAs FET amplifier module with gate periphery of 12 mm, has been developed with 6 watt output power at 6 GHz with associated gain of 9 dB. The last paper of this session describes a new GaAs high power FET developed by F. Fukaya et al. This FET chip of 10.8 mm gate-width employs deep recess, via hole PHS, air-bridged gate-source cross-over and novel gate feed network technology. The internally matched device which consists of two chips (gate-width of 21.6 mm) has demonstrated 10 watt of the 1 dB gain compression power with 8 dB gain and 43% power added efficiency at 8 dB.

0149-645X/84/0000-0187 $01.00 © 1984 IEEE